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In re Patent Application of

: Atty. Docket No. POU920010165US1

Marvin J. RICH et al.

: Group Art Unit: 2825

Serial No. 10/038,209

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**For: *DELAY CORRELATION ANALYSIS AND REPRESENTATION
FOR VITAL COMPLIANT VHDL MODELS***

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SUBMISSION OF FORMAL DRAWINGS

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Submitted herewith are 22 sheets of formal drawings containing Figures 1-22 for the above-identified application.

The Commissioner is authorized to charge any additional fees or credit any overpayment to Deposit Account No. **09-0463**.

Respectfully submitted,

Date:

3/27/02

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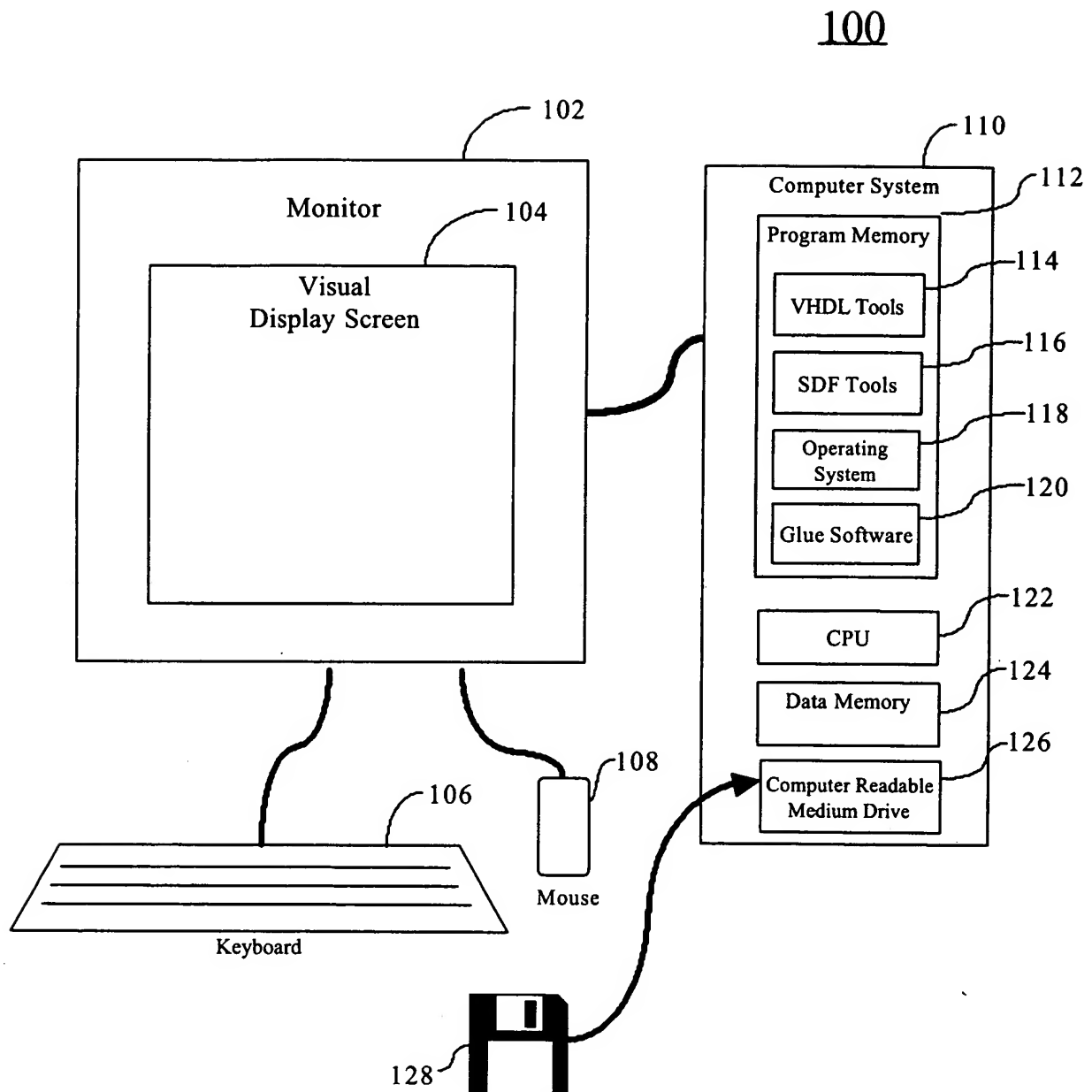


FIG 1

112

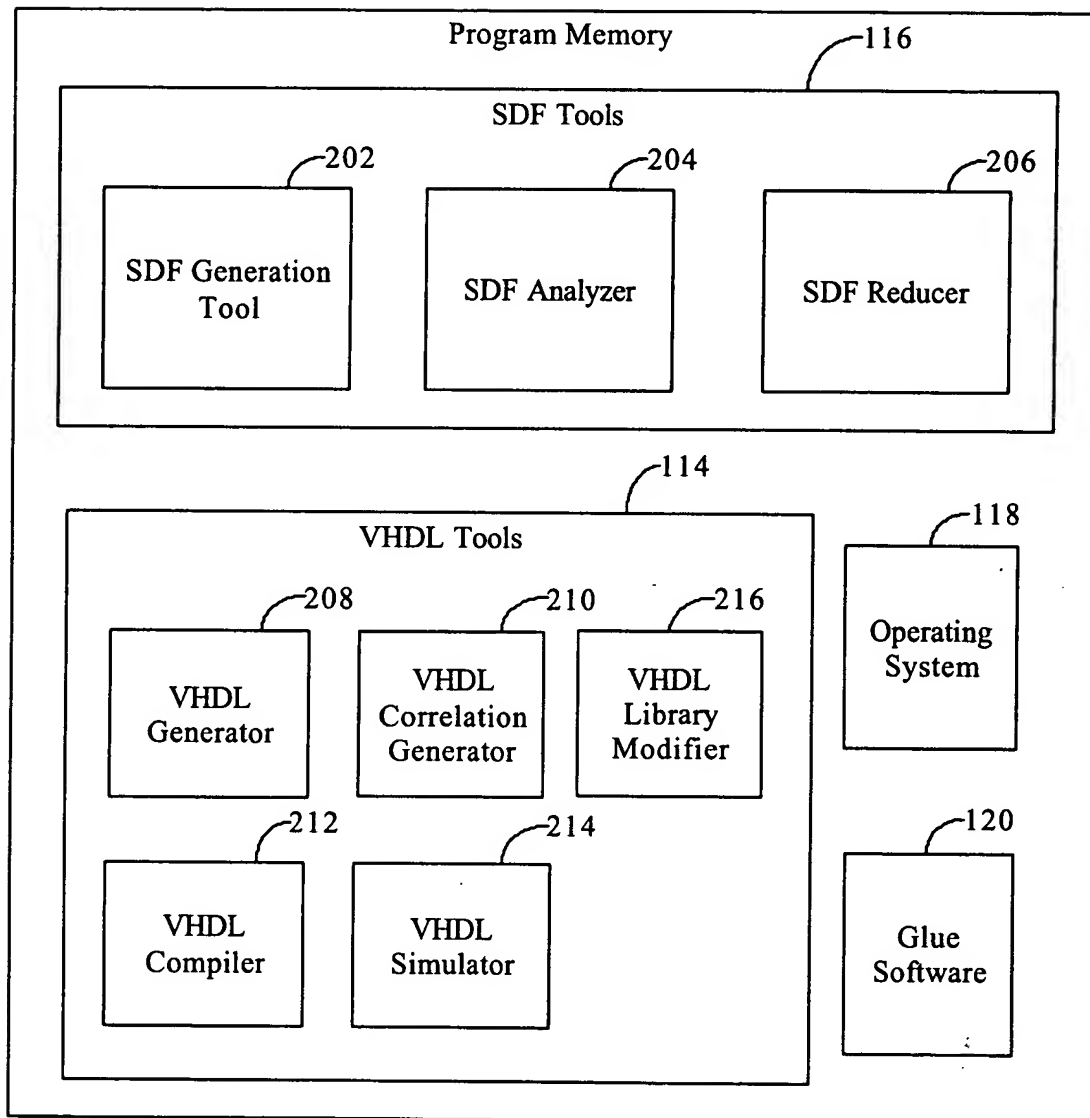


FIG 2

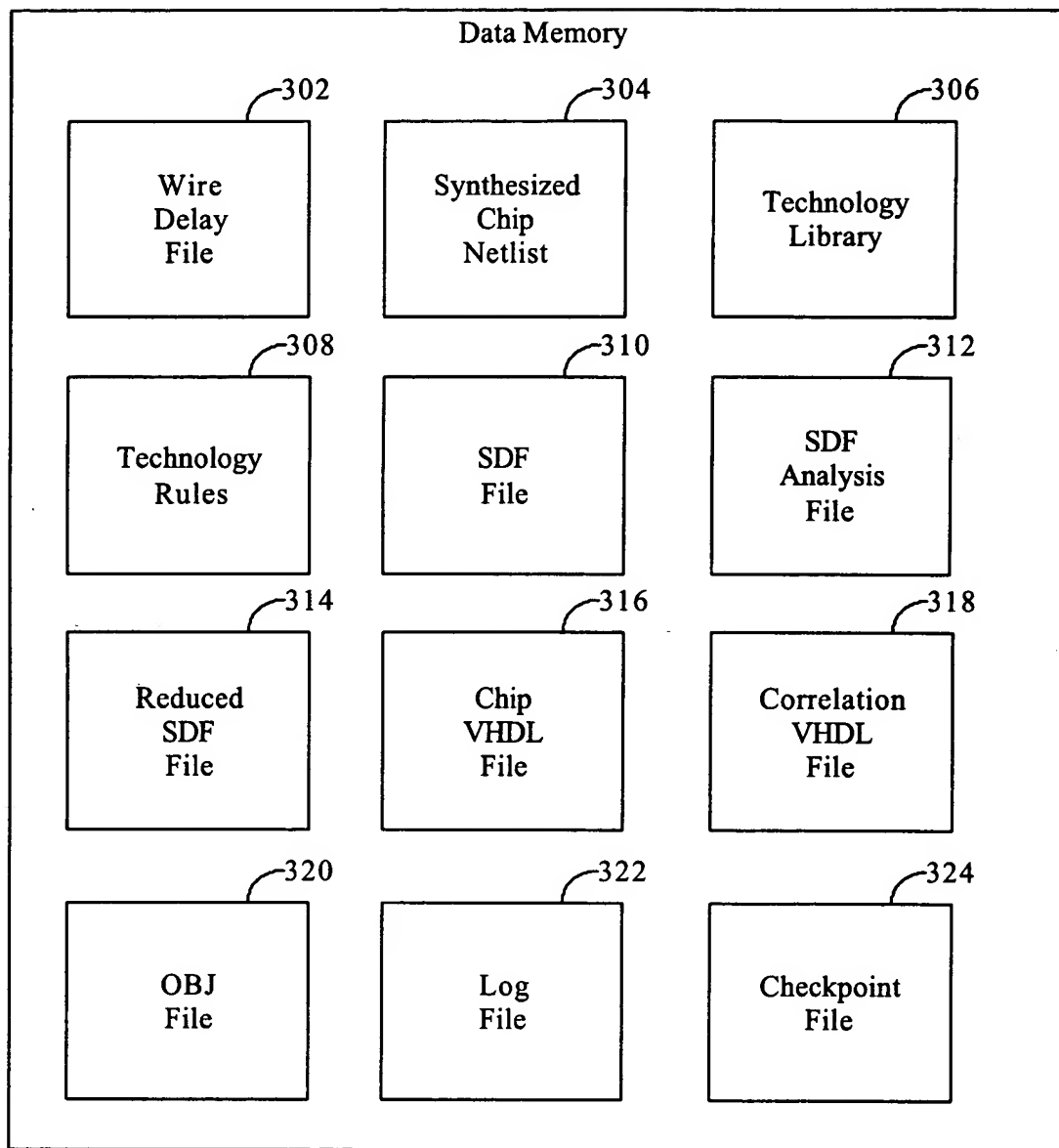


FIG 3

400

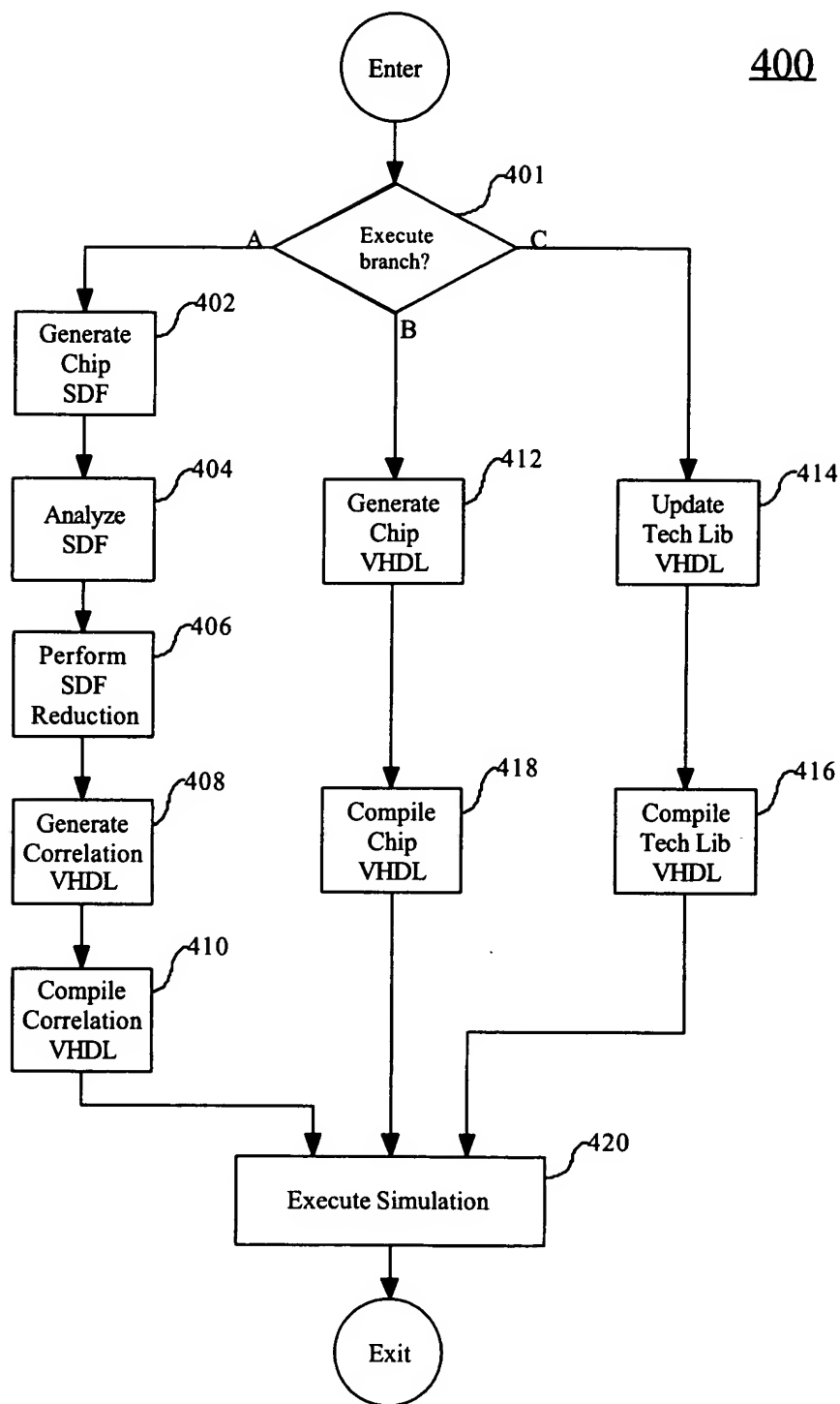


FIG 4

402

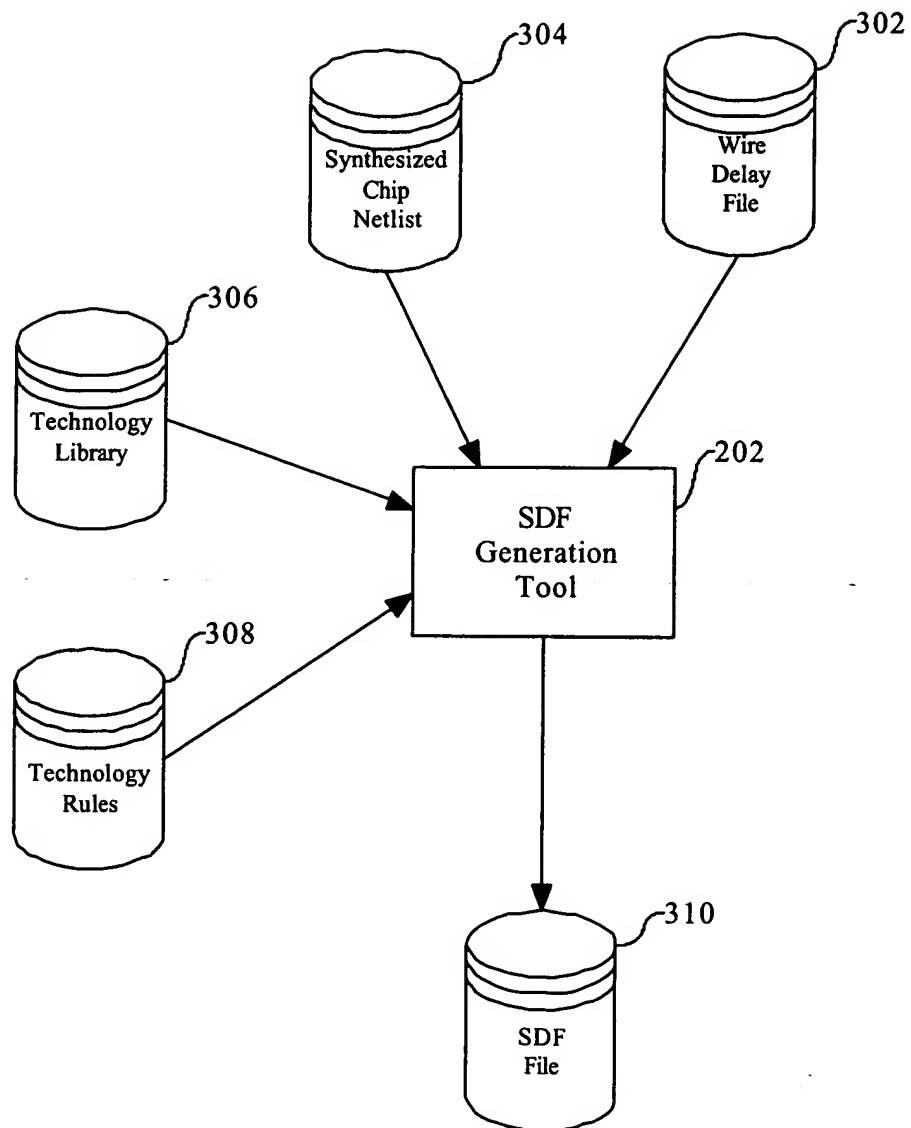


FIG 5

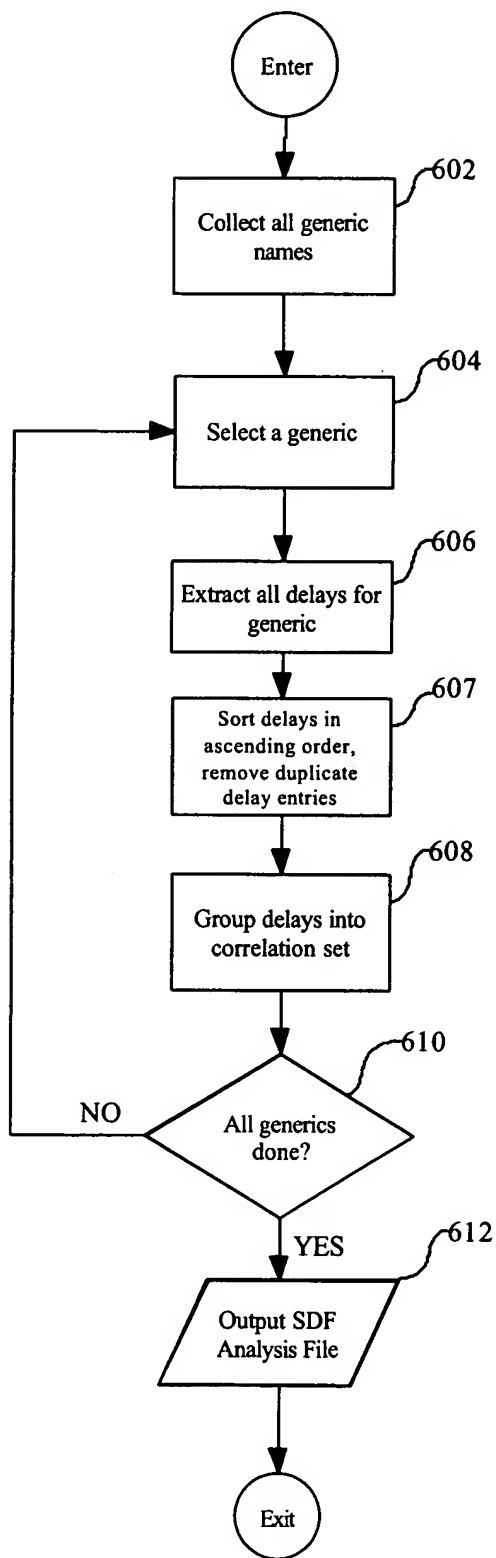


FIG 6

700

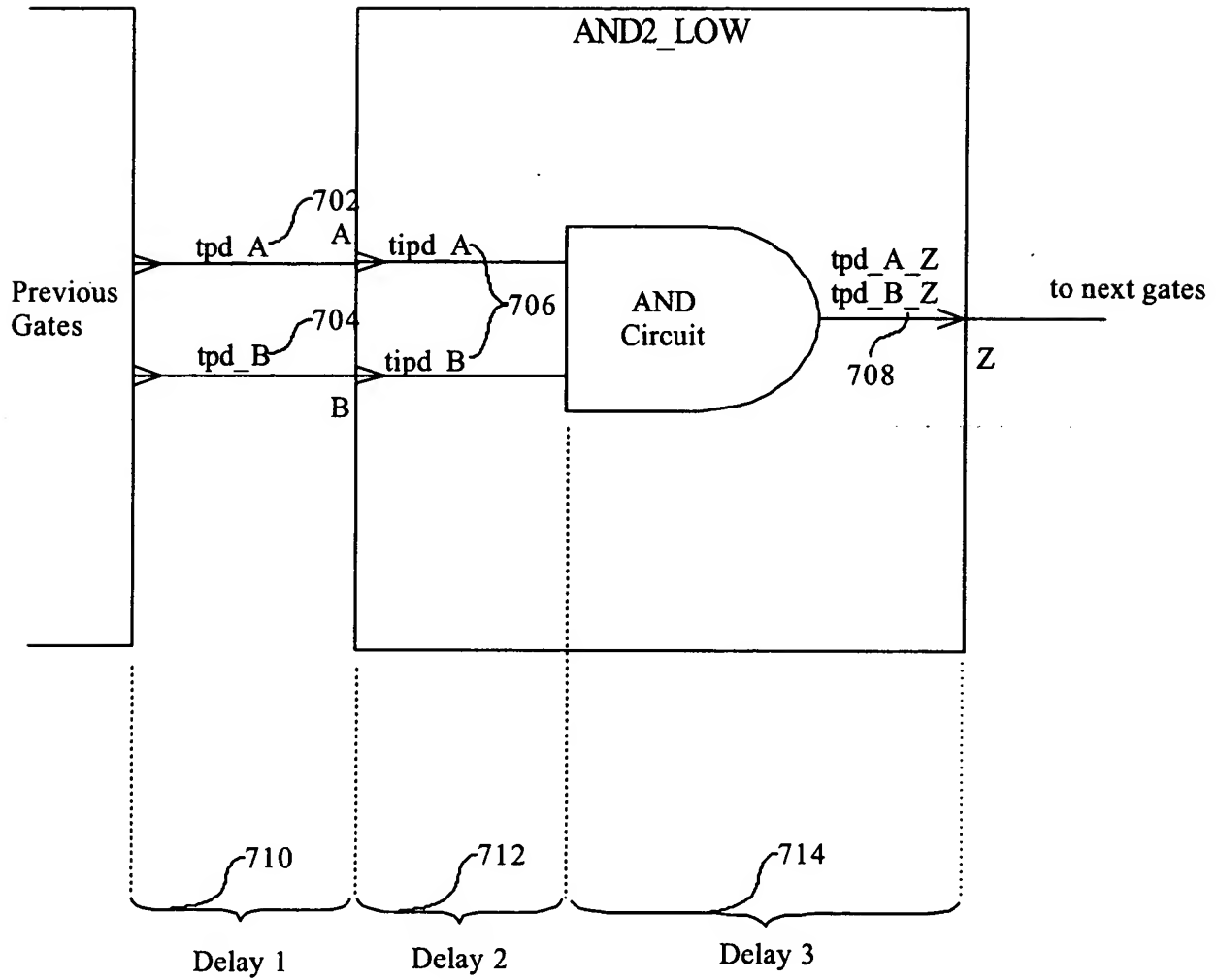


FIG 7

800

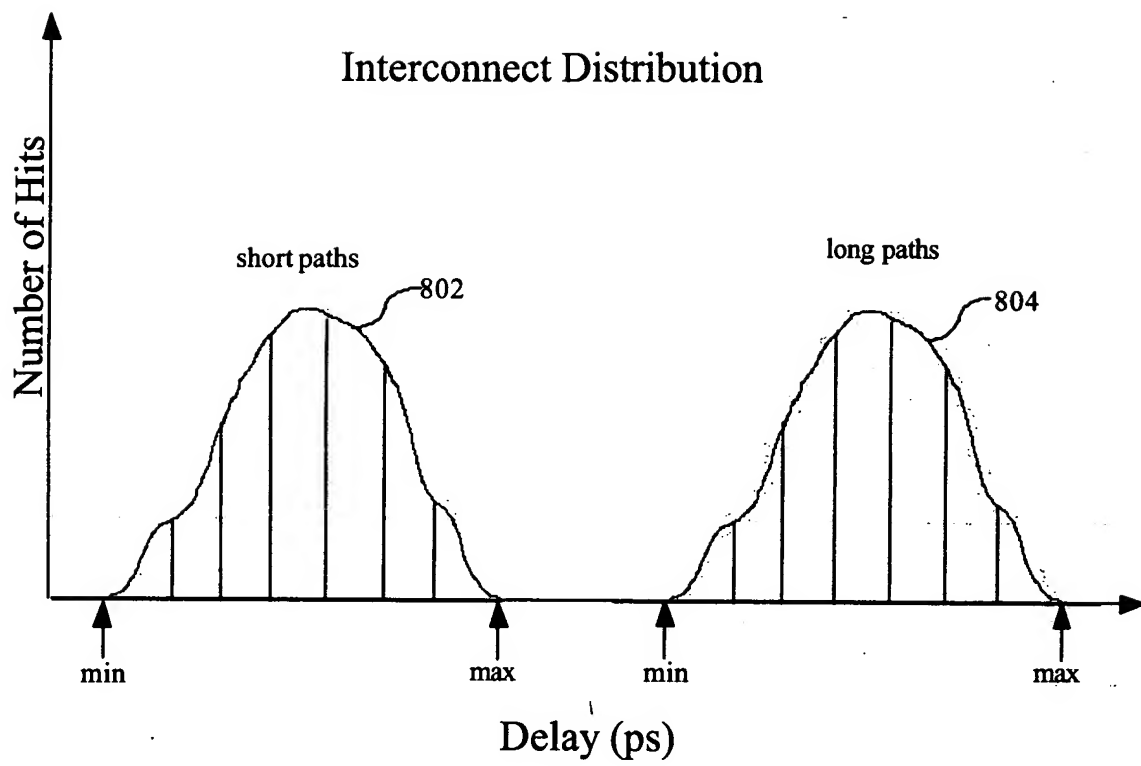


FIG 8

900

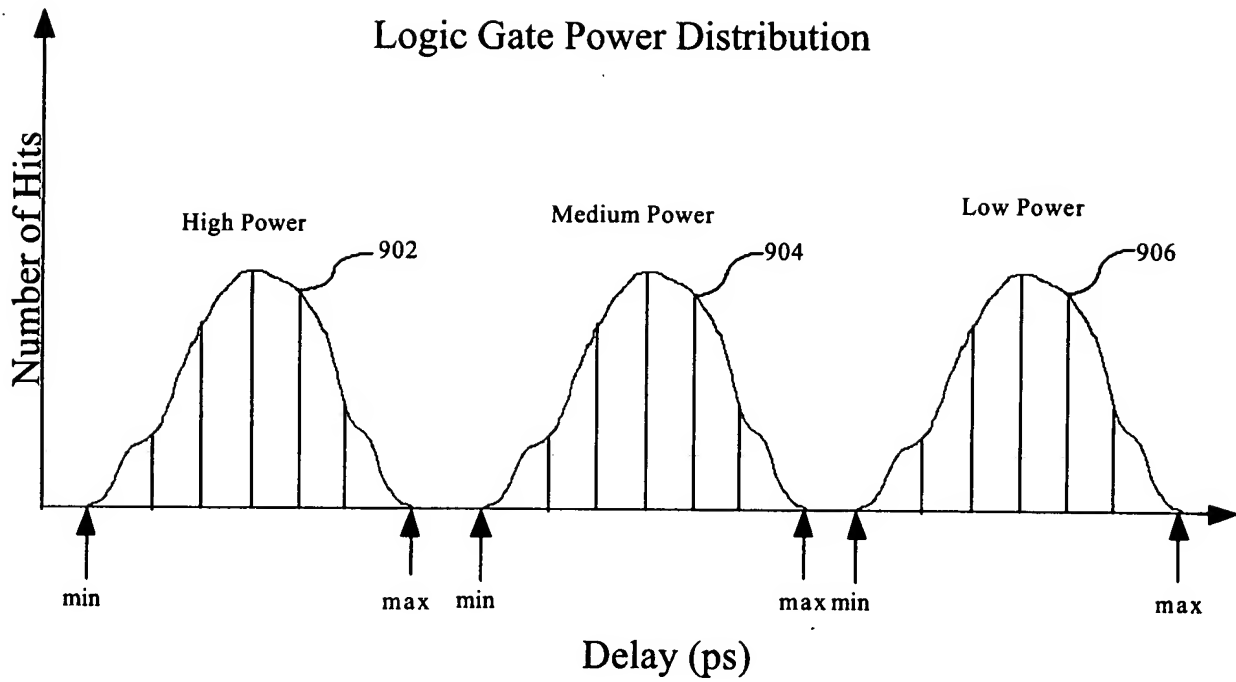


FIG 9

1000

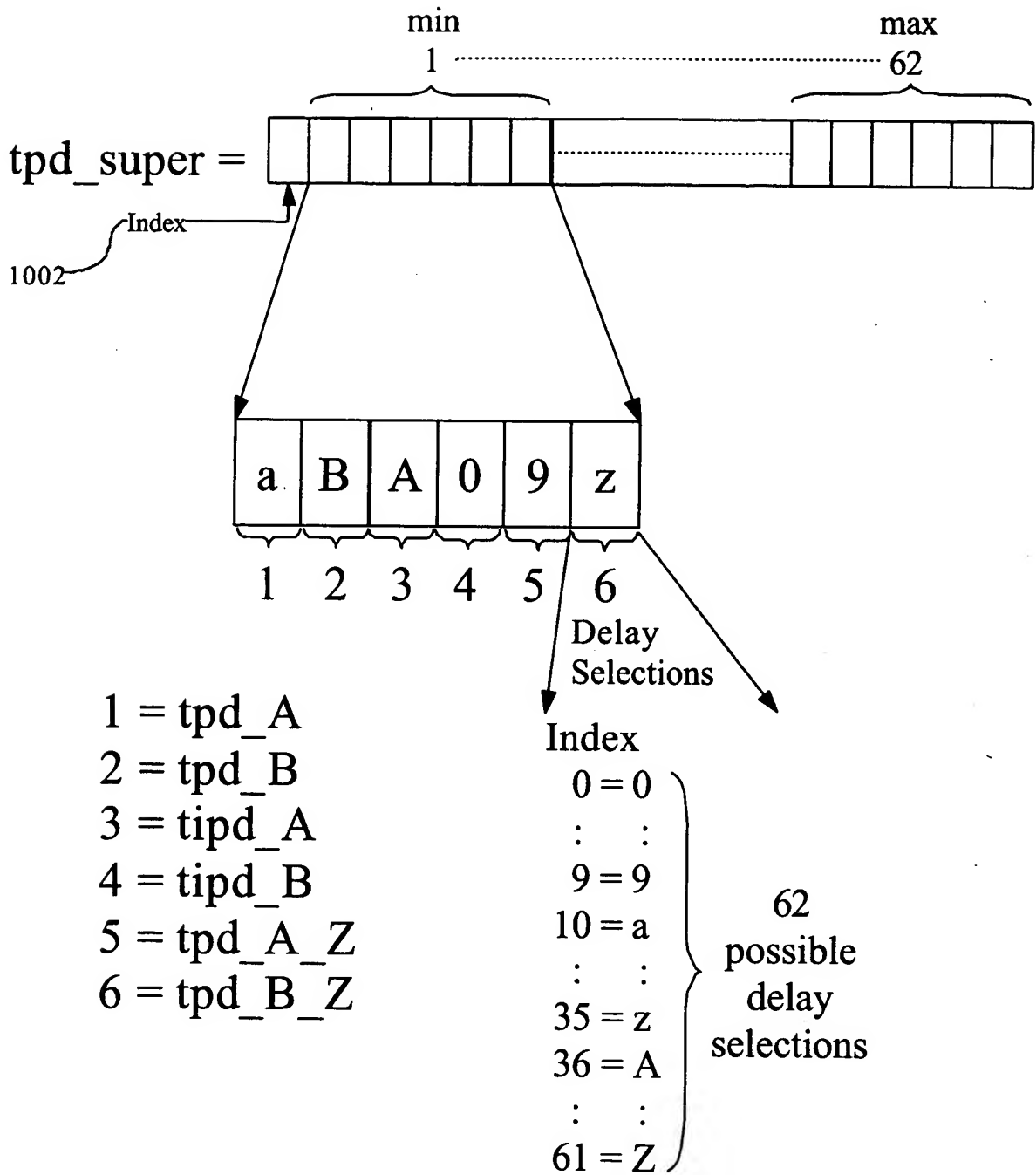


FIG 10

1100

Correlation Table

BOOK_TYPE	MAPS TO	SET SIZE
•		
•		
•		
AND2_MED	AND2_NEW	6
•		
•		
•		

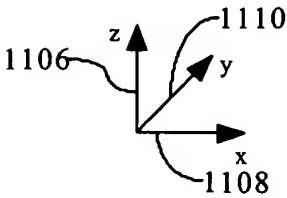
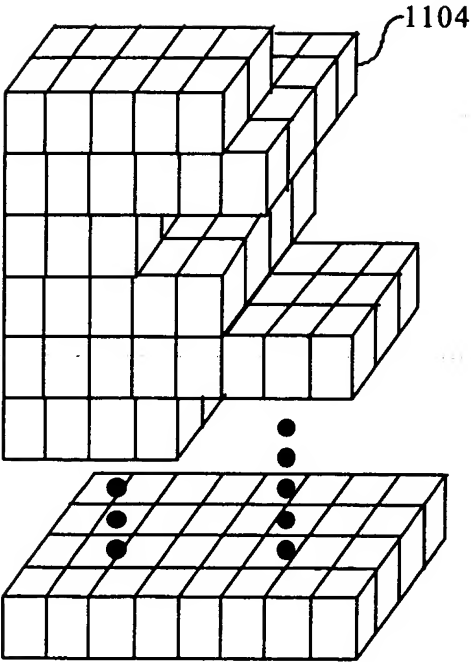
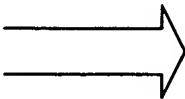


FIG 11

1200

CHAR POSITION (0 OFFSET)	CHAR VALUE	Correlation Set (x')	Entry Position (y')	Slot Offset (x'')
0	1	NA	NA	NA
1	4	1	5th	1st
2	X	1	60th	2nd
3	a	1	11th	3rd
4	m	1	26th	4th
5	p	1	29th	5th
6	l	1	25th	6th

FIG 12

206010 603030

1300

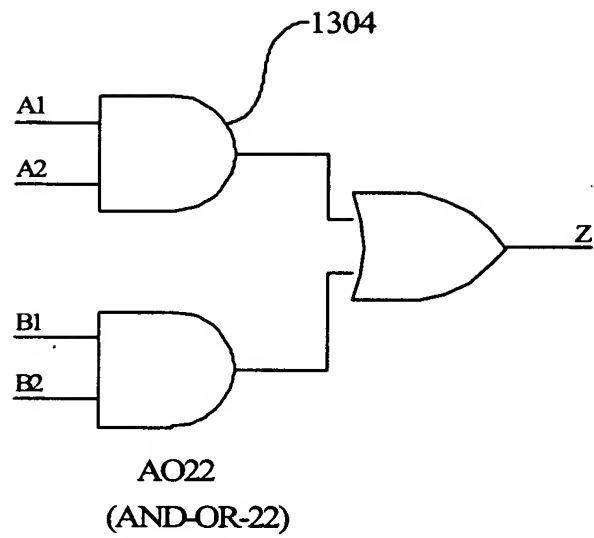
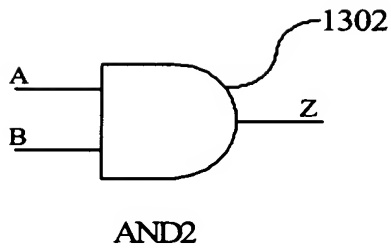
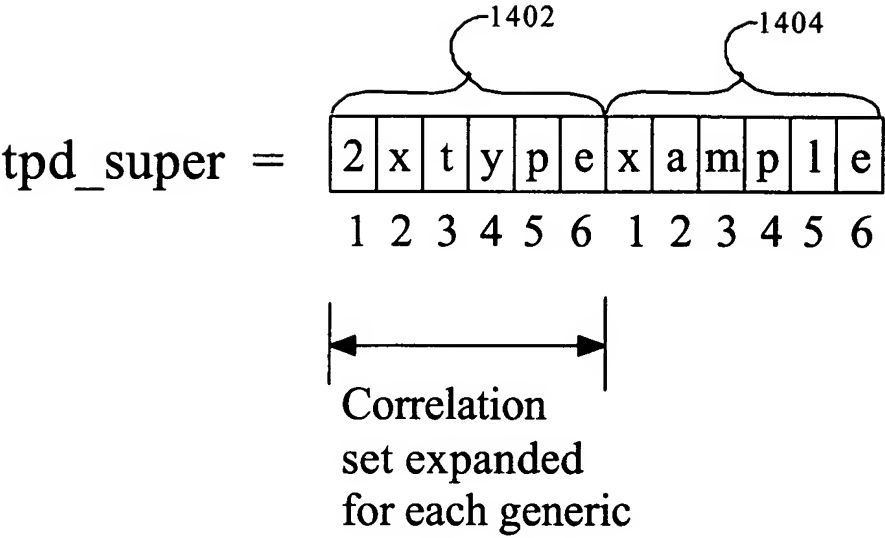


FIG 13

1400



- 1 → tpd_A
- 2 → tpd_B
- 3 → tipd_A
- 4 → tipd_B
- 5 → tpd_A_Z
- 6 → tpd_B_Z

FIG 14

1500

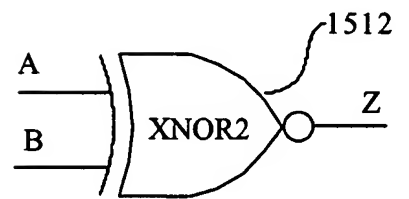
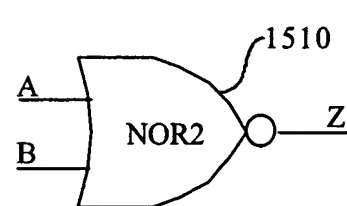
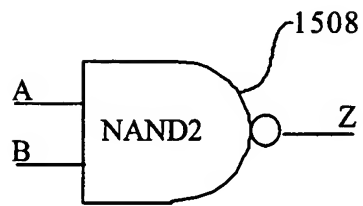
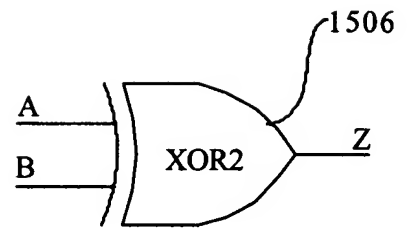
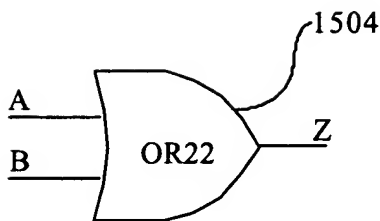
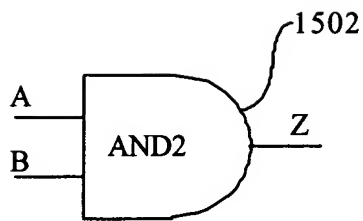
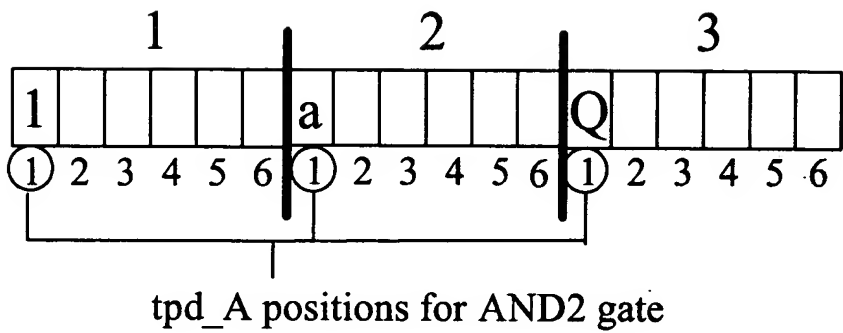


FIG 15

1600



Encode as:

DELAY	tpd A		
DELAY	1	2	3
-0.500 ns	0	0	0
-0.499 ns	0	0	1
+237.826 ns	Z	Z	Y
+237.827 ns	Z	Z	Z

FIG 16

1700

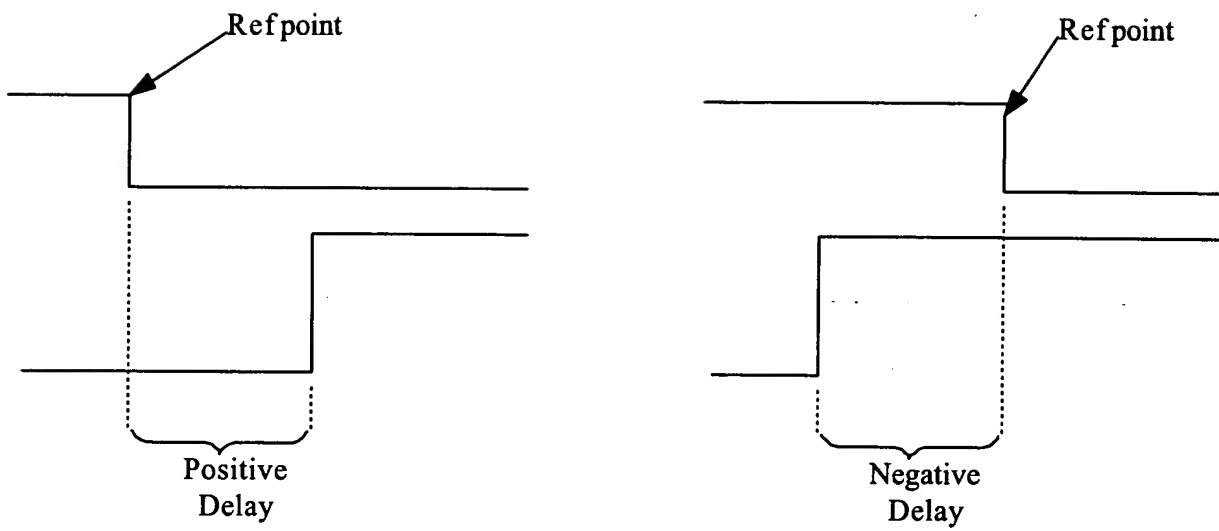


FIG 17

406

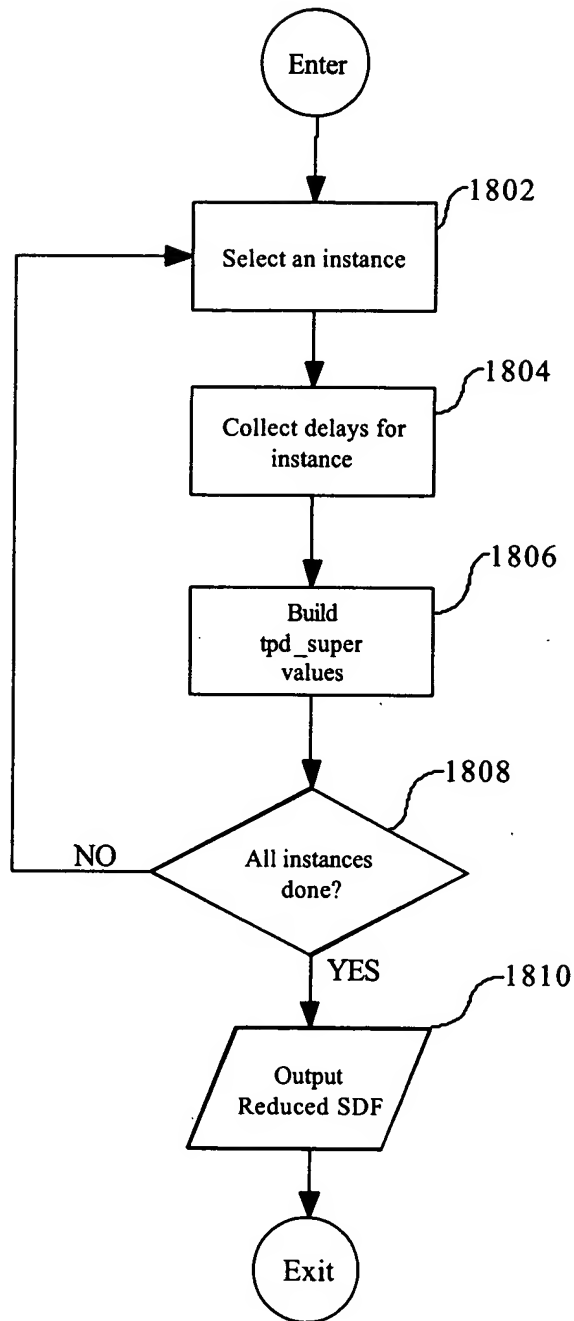


FIG 18

408

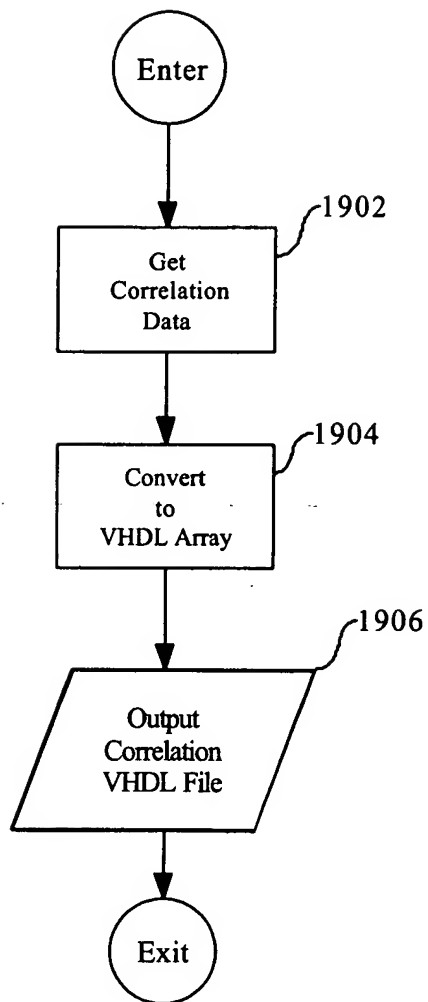


FIG 19

412

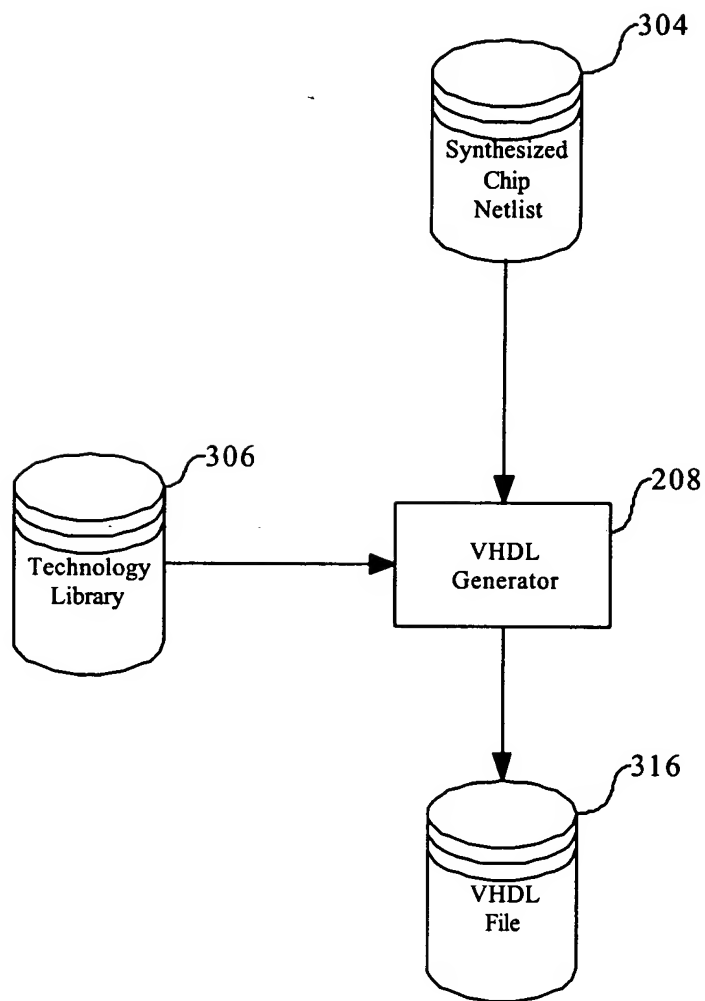


FIG 20

418

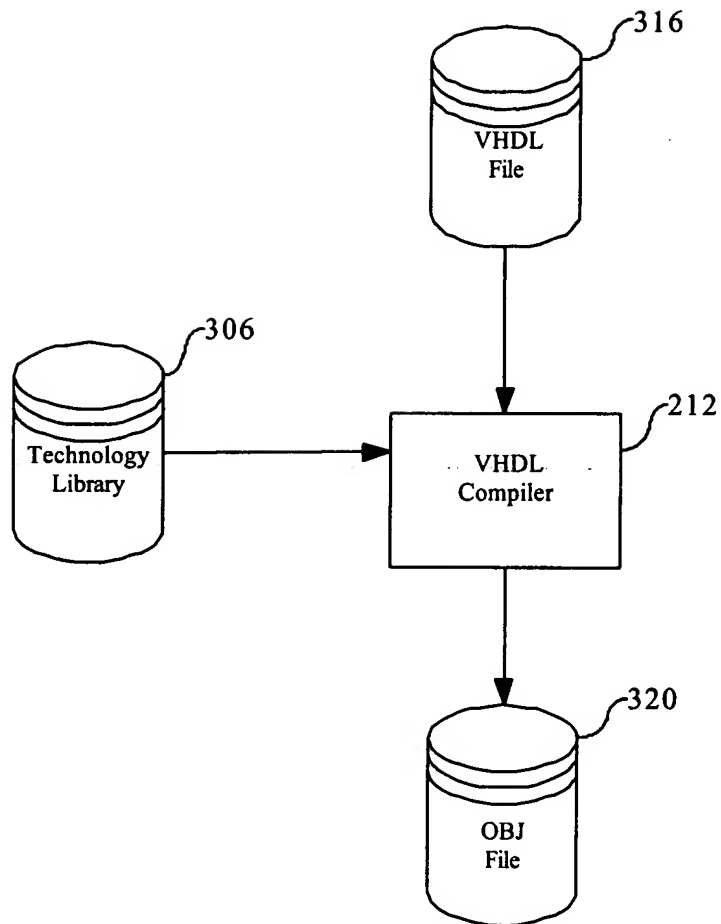


FIG 21

420

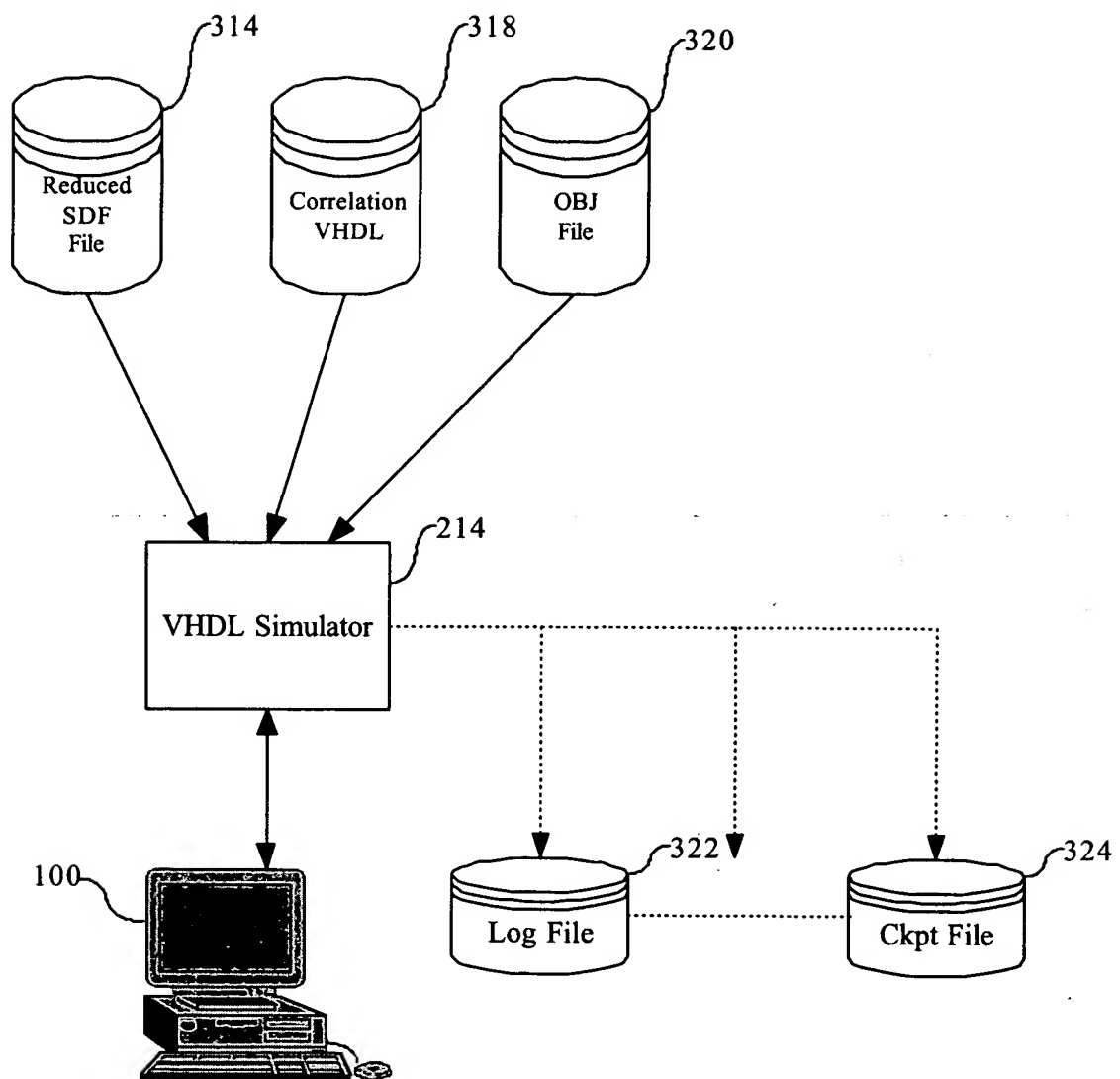


FIG 22